



Microsystems Packaging & Interconnect Roadmap

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Presentation for final technical review
Lancaster 2007

Dec-07

«Design for Micro & Nano Manufacture (NoE PATENT-DfMM)»
Network of Excellence funded by the European Commission (EC FP6: IST, Unit C2, Contract 507255)

- ❑ Partners involved
- ❑ Definition and benefits
- ❑ Objectives of project
- ❑ Previous roadmaps and examples
- ❑ Methodology used
- ❑ Results
- ❑ Conclusions



- Heriot-Watt University (UK):
Leader



- IZM Berlin (D): Co-organiser of
meetings



- QinetiQ (UK): Co-investigator



- 4M2C (D): Co-investigator

- ❑ Technology Roadmapping is a process by which the timescale for future technologies and capabilities can be presented in a diagrammatic or tabular format to describe a future vision.
- ❑ When read in conjunction with the requirements of a particular organisation, the roadmap helps to identify technologies and capabilities that are critical to realising a future vision.
- ❑ Using roadmapping techniques with a group of experts brings about the emergence of a common vision and the main barriers to achieving this vision.

- Collect information regarding current and future trends of packaging using focused questionnaires and technology roadmapping techniques during **two dedicated and facilitated workshops**.
- Deliver a technology roadmap for packaging containing these key developments and their timescale for realisation, together with an idea of their priority for the Virtual Laboratory to tackle them.
- Agree on a common vision of the field of packaging, and therefore facilitate the uptake of MEMS by focussing on key problems.
- This roadmap (52 pages documents, April 2007) are to be used by the PATENT management committee to translate the common vision into key initiatives for the DfMM-PATENT community to target its efforts on and over which timescales, as well as key gaps and best practice for the Virtual Laboratory in order to better serve the industry in the long run.
- The outputs of this project will therefore constitute a precious resource for the future PATENT Business Plan.

- ❑ Fraunhofer IZM packaging roadmap (semiconductors)
- ❑ ITRS roadmap, containing a packaging section (semiconductors)
- ❑ The NEXUS roadmap (MEMS)
- ❑ The MANCEF roadmap (MEMS)
- ❑ MEMSTAND roadmap
- ❑ PIDEA roadmap (semiconductors, with some elements of MEMS)
- ❑ And various other roadmaps from the internet.

Conclusions about existing roadmaps

- ❑ Very few technical details. Most of the MEMS roadmaps are fairly high-level and give interesting market forecasts, but do not tackle technology developments and R&D activities.
- ❑ However, the format of several roadmapping elements such as tables or diagrams was deemed very usable by the project partners, especially from the ITRS roadmap (Challenges, Technology Requirement tables) and the Senscope Roadmap

Table 4: Packaging Challenges through 2007

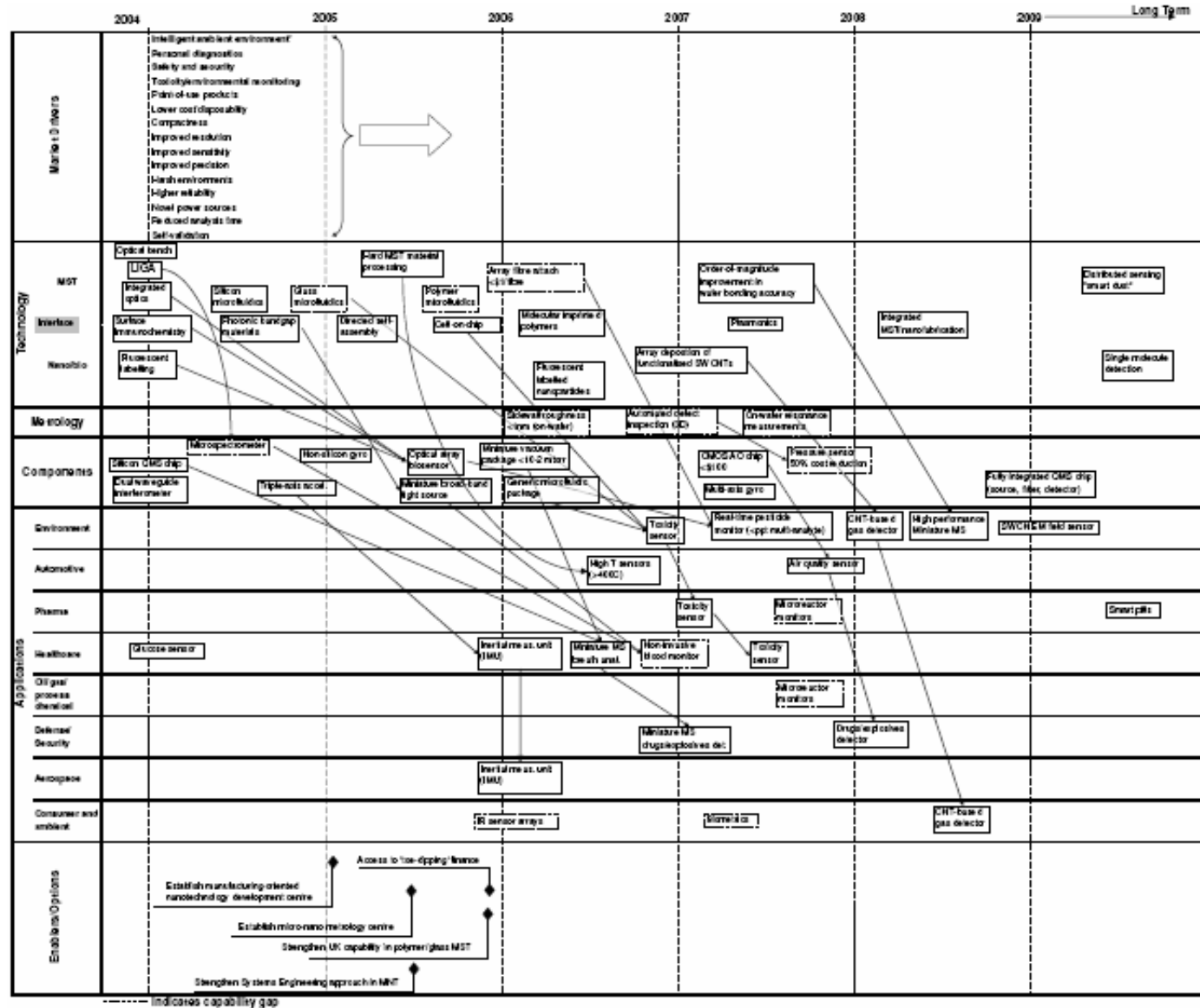
| Difficult Challenges (Through 2007) | Summary of Issues |
|---|---|
| Improved organic substrates | T _g (Glass Transition Temp.) compatible with lead-free solder processing |
| | Increased wireability at low cost, substrates are a barrier to flip chip adoption |
| | Improved impedance control and lower dielectric loss to support higher frequency applications |
| | Improved planarity and low warpage at higher process temperatures |
| | Low moisture absorption |
| | Low-cost embedded passives |
| Improved underfills for flip chip on organic substrates | Improve flow, fast dispense/cure, better interface adhesion, lower moisture absorption |
| | Higher operating range for automotive and Pb free soldering in liquid dispense underfills |
| | Improved adhesion, small filler size, and improved flow for mold based underfills |
| Coordinated design tools & simulators to address chip, package, and substrate co-design | Chip, package, and system level co-design tools |
| | Educational programs required to train engineers in co-design technologies |
| | Faster analysis tools for integrated thermal mechanical analysis |
| | Higher accuracy, faster electrical simulation capability for high frequency design |
| Impact of Cu/low κ (dielectric constant) on packaging | Direct wirebond and bump to Cu (Copper) |
| | Bump & underfill technology to assure low κ dielectric integrity |
| | Improved Mechanical strength of dielectrics |
| | Interfacial adhesion |

Table 93a Single-chip Packaging Technology Requirements—Near-term *UPDATED*

| Year of Production | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 |
|--|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Technology Node | | 90nm | | | 65nm | | |
| DRAM to Pitch (nm) | 100 | 90 | 80 | 70 | 65 | 57 | 50 |
| Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin) | | | | | | | |
| WAS Low-cost, hand-held and memory | 0.30-0.68 | 0.28-53 | .27-50 | .28-48 | .26-45 | .23-43 | .22-41 |
| IS Low-cost, hand-held and memory | -- | 0.30-53 | .27-50 | .28-48 | .26-45 | .23-43 | .22-41 |
| WAS Cost-performance | .75-1.30 | .71-1.24 | .87-1.17 | .84-1.11 | .81-1.05 | .68-1.00 | .66-98 |
| IS Cost-performance | -- | .71-1.24 | .87-1.17 | .84-1.11 | .81-1.05 | .68-1.00 | .66-98 |
| High-performance | 1.88 | 1.88 | 1.78 | 1.88 | 1.81 | 1.62 | 1.45 |
| WAS Harsh | 0.38-3.20 | 0.32-2.88 | 0.28-2.80 | 0.28-2.33 | 0.23-2.11 | 0.21-2.00 | 0.20-1.80 |
| IS Harsh | -- | 0.32-2.88 | 0.28-2.80 | 0.28-2.33 | 0.25-2.11 | 0.23-2.00 | 0.22-1.90 |
| Chip Size (mm ²) [3] | | | | | | | |
| Low-cost | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| Cost-performance | 140 | 140 | 140 | 140 | 140 | 140 | 140 |
| High-performance | 310 | 310 | 310 | 310 | 310 | 310 | 310 |
| Harsh | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| Maximum Power (Watts/mm ²) [4] | | | | | | | |
| Low-cost (Watts) [1] | 2.5 | 2.7 | 2.8 | 3 | 3 | 3 | 3 |
| Cost-performance | 0.57 | 0.8 | 0.85 | 0.7 | 0.74 | 0.78 | 0.83 |
| High-performance | 0.48 | 0.61 | 0.54 | 0.58 | 0.61 | 0.64 | 0.64 |
| Harsh | 0.14 | 0.18 | 0.18 | 0.18 | 0.18 | 0.2 | 0.2 |
| Core Voltage (Volts) | | | | | | | |
| Low-cost | 1.2 | 1.2 | 1 | 0.9 | 0.9 | 0.8 | 0.8 |
| Cost-performance | 1.2 | 1.2 | 1 | 0.9 | 0.9 | 0.8 | 0.8 |
| High-performance | 1.2 | 1.2 | 1 | 0.9 | 0.9 | 0.8 | 0.8 |
| Harsh | 2.5 | 2.5 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| Package Pincount Maximum [5][6] | | | | | | | |
| Low-cost | 112-408 | 122-500 | 134-550 | 144-800 | 160-880 | 180-720 | 180-300 |
| Cost-performance | 600-1462 | 500-1800 | 550-1780 | 550-1938 | 800-2140 | 800-2400 | 880-2800 |
| High-performance | 2400 | 3000 | 3400 | 3800 | 4000 | 4400 | 4800 |
| Harsh | 450 | 600 | 660 | 800 | 880 | 720 | 780 |
| Minimum Overall Package Profile (mm) | | | | | | | |
| WAS Low-cost | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 |
| IS Low-cost | 0.5 | 0.5 | 0.4 | 0.4 | 0.4 | 0.4 | 0.4 |
| Cost-performance | 1 | 0.8 | 0.8 | 0.8 | 0.8 | 0.85 | 0.85 |
| High-performance | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Harsh | 1 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 |
| Performance: On-Chip (MHz)[7] | | | | | | | |
| WAS Low-cost | 602/3184 | 552/3514 | 607/3885 | 888/4251 | 736/4878 | 800/5000 | 830/5150 |
| IS Low-cost | 602/3184 | 552/5200 | 607/3885 | 888/4251 | 736/4878 | 800/5000 | 830/5150 |
| Cost-performance | 3080 | 3880 | 5170 | 6830 | 8740 | -- | -- |
| High-performance | 3080 | 3880 | 5170 | 6830 | 8740 | -- | -- |
| Harsh | 72 | 80 | 88 | 96 | 108 | 116.8 | 128.28 |

Note: Maximum power is average for die area

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known



- Phase 1
 - Create a first draft of a "High-Level Challenges and Related Issues" table, on the model of the ITRS roadmap
 - *Step 1:* read existing literature on packaging, including some PATENT deliverables and create a first draft table.
 - *Step 2:* prepare a questionnaire and send it to a list of packaging experts to expand on the draft table.
 - Outcome: draft table analysed by the project partners individually and issues were classified under the 11 High-Level Challenges.

11 high level challenges

- ❑ Low-cost Hermetic/vacuum packaging & Low-cost alternatives to hermetic packaging (near hermetic, plastic packages...)
- ❑ Low-cost Wafer Level Packaging
- ❑ Improvements in CAD/Modelling
- ❑ Stress management to keep induced torsions as low as possible
- ❑ Monolithic integration (active drive electronics, 3D stacking, System on Chip, Via technologies...)
- ❑ Hybrid Integration (System in a Package, passive integration, Chip on Board, Via technologies...)
- ❑ Built-in monitoring, Smart packages
- ❑ Improved interfacing of MEMS device (optical assembly, active and passive alignment, soldering techniques)
- ❑ Improved reliability (signal management, noise, interferences, interconnection reliability...)
- ❑ Future packages (flexible substrates, chip in polymer no package...)

- Phase 2: Organise workshops (HWU, April 2006; Berlin June 2006) to reach a common vision on packaging challenges
 - *Purpose:* finalise the draft list of High-Level Challenges and Related Issues to get to a common view shared by industrialists and academics.
 - 30 participants, 15 from industry.
 - Stage 1: Discuss the High-Level Challenges
 - Stage 2 : Discuss related issues under each High-Level Challenge. 150 issues in total.
 - Stage 3: Prepare next workshop (Berlin, June 2006). Focus on 4 challenges following second questionnaire
- Phase 3 : Produce a roadmap following the two workshops

- 11 challenges refined:
 - Hermetic/vacuum packaging and low-cost alternatives (near hermetic, plastic packages...)
 - Low-cost Wafer Level Packaging and related testing techniques
 - Improvements in CAD/Modelling
 - Stress management to keep induced deformations (torsions, bending, buckling...) as low as possible
 - 3D stacking and monolithic integration
 - Hybrid Integration (System in a Package, passive integration, Chip on Board, interconnections and flip-chip technologies...)
 - Built-in monitoring, Smart packages
 - Improved interfacing of MEMS device (optical assembly, active and passive alignment, soldering techniques)
 - Improved reliability (signal management, noise, interferences, interconnection reliability...)
 - Future packages (flexible substrates, chip in polymer no package...)
 - Application Specific packages (e.g. bio, opto applications)

- **Short / Medium / Long term (S,M,L):**
 - corresponds to your perception of when the technology will reach a reasonable maturity. Short term: before 2008, Medium term: 2010, Long term: after 2010

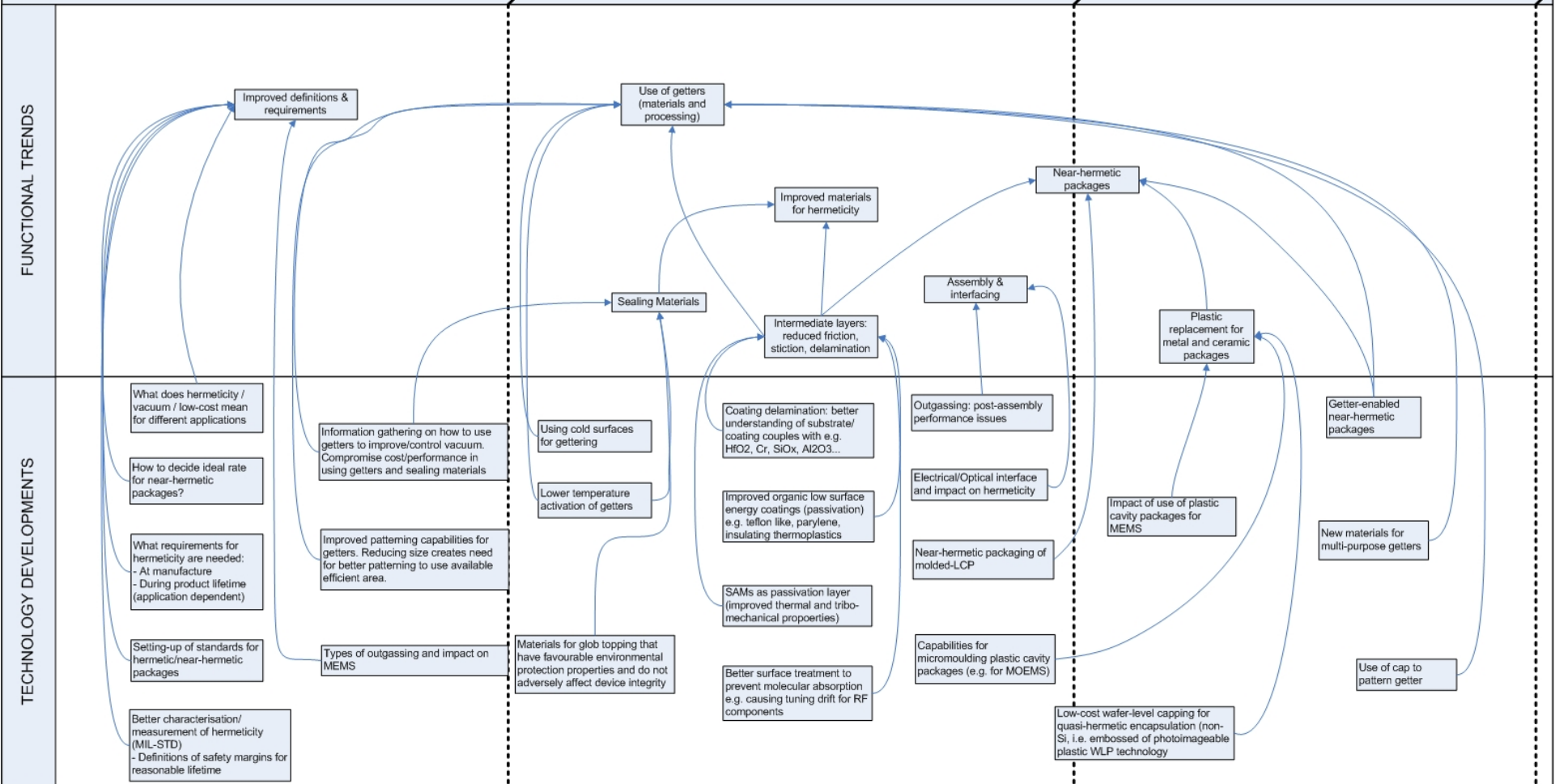
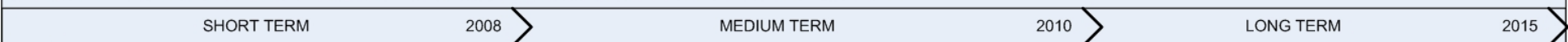
- **High, Medium, Low priority (H,M,L):**
 - corresponds to your perception of the impact of tackling this particular issue on the take up of MEMS

- **RF / MOEMS / Both:**
 - specific to RF MEMS, MOEMS or both

Results An example

| | Term (S/M/L) | Priority (L/M/H) | RF/O/Both |
|--|--------------|------------------|-----------|
| High Level Challenges and related issues | | | |
| Hermetic/vacuum packaging and low-cost alternatives (near hermetic, plastic packages...) | | | |
| Clarification of definitions (what is hermeticity, vacuum, low cost?) | S | H | B |
| OUTGASSING: Impact of outgassing / post assembly performance issues Type of outgassing and Impact on MEMS Control of outgassing (getter on "cold" surfaces, and again: device and application dependent) | M | M | B |
| What level of hermeticity is needed (mbar l s-1) (1) at manufacture and (2) during product lifetime (device dependent/application dependent). How to decide ideal rate for near hermetic packages? | M | H | B |
| How to characterise/measure hermeticity (Mil-STD)? Definitions of safety margin for reasonable life time and setting up of standards for hermetic/near-hermetic packaging | S | H | B |
| Information gathering on how to use getters to improve / control vacuum. In particular: impact of getters and sealing materials: compromise performance/cost | S | H | B |
| Patterning capabilities for getters (deposition of materials): getters are conductive, so reducing size creates need for better patterning to use available area efficient. For instance, shadow masking will not be sufficient anymore when reducing the size for RF switches below 1x1mm total area of CSP | S | H | B |
| Getters: temperature of activation affecting MEMS | M | L | B |
| Use of cap to pattern getter (thin-film getter) | L | L | B |
| New packaging materials for multi-purpose (e.g. moisture particle) getters | L | M | B |
| Getter-enabled near hermetic packages | | | |
| Near hermetic packaging of molded LCP | | | |
| Impact of use of plastic cavity packages for MEMS / Plastic replacement for ceramic & metal packages | M | H | B |
| Capabilities for micromolding plastic cavity packages for MOEMS | M | H | O |
| Low cost wafer level capping for quasi-hermetic encapsulation (non-silicon, i.e. embossed or photo-imageable plastic WLP technology) | M | H | B |
| Sealing materials (application dependent, e.g. space, bio-medical, transmissive packaging media...) | S | H | B |
| Electrical/optical interface and impact on hermeticity | M | M | B |
| Surface treatment of structures to prevent molecular absorption causing tuning drift for RF components to reduce need for package requirements | S | H | RF |
| Improved organic low surface energy coating (teflon like, parylene, insulating thermoplastic coatings...) | S | H | B |
| Improved Self-Assembled Monolayers (SAMs) as passivation coatings (improved thermal and tribo-mechanical properties) | S | H | B |
| Intermediate bonding layer: Better understanding of substrate/coating couples with HfO ₂ , Cr, SiO _x , Al ₂ O ₃ ... | M | M | B |
| Materials for "glob topping" that have favourable environmental protection properties and do not adversely affect the device integrity | S | M | O |
| Low-cost Wafer Level Packaging | | | |
| Information on the worldwide status of WLP – understand pros and cons of various techniques | S | M | B |
| Low cost = high vol, automation issues | M | H | B |
| Yield optimisation, quality | L | H | B |
| Cavity atmosphere and control | M | M | B |
| Assessment techniques: suitable wafer level testing/characterisation, in particular (ex-situ) testing of wafer-level packaging is not yet fully solved | S | H | B |

HERMETIC/VACUUM PACKAGING AND LOW-COST ALTERNATIVES (NEAR HERMETIC, PLASTIC ...)



- ❑ An excellently managed activity under WP7 with industrial buy-in and academic take up.
- ❑ Good methodology whose results could have been refined with additional workshops.
- ❑ A wealth of results to be analysed closely that can feed into National and European projects.